REMARKS

The Office Action dated April 11, 2002, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

By this Amendment, claims 1-6, 8, 10-15, 17 and 19-23 have been amended. No new matter has been added by the amendments. Accordingly, claims 1-23 are pending in this application and are respectfully submitted for consideration.

Figures 1-2 of the Drawings have been objected to. The Examiner states that Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. The Drawings have been amended per the Examiner's suggestion to add the legend --Prior Art--. Thus, withdrawal of the rejection is respectfully requested.

The Abstract of Disclosure in the Specification has been objected to for informalities. A new Abstract of the Disclosure is included, as shown on the attached sheet, correcting the informalities. Thus withdrawal of the objection is respectfully requested.

Claims 6, 8, 15 and 17 have been rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 6, 8, 15 and 17 have been amended to overcome this rejection. Thus, withdrawal of the rejection is respectfully requested.

Claims 1-4, 6, 8-13, 15 and 17-23 have been rejected under 35 U.S.C. §102(e) as being anticipated by Ilkbahar (U.S. Patent No. 6,026,456). The rejection is

respectfully traversed because Ilkbahar fails to disclose, teach or suggest each and every element recited in the rejected claims.

Claim 1 recites a termination resistor circuit, provided in an interface circuit through which signals are transferred. Claim 1 recites that the termination resistor circuit includes a first termination resistor block having a plurality of transistors with a same logic voltage being applied to gates of the transistors of said first termination resistor block. Claim 1 also recites that the termination resistor circuit includes a second termination resistor block having a plurality of transistors with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block, wherein said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

Among other features, claims 10, 19 and 23 (like claim 1) all recite a first termination resistor block having a plurality of transistors with a same logic voltage being applied to gates of the transistors of said first termination resistor block, and a second termination resistor block having a plurality of transistors with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block.

Ilkbahar fails to disclose, teach or suggest a first termination resistor block having a plurality of transistors with a same logic voltage being applied to gates of the transistors of said first termination resistor block, and a second termination resistor block having a plurality of transistors with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration

from said first termination resistor block as recited in claims 1, 10, 19 and 23.

Ilkbahar merely discloses a termination circuit which comprises a first and a second pullup device. The first pullup is a transistor 560, and the second pullup is a plurality of transistors represented as a pullup 540. The transistor 560, a N channel MOS transistor, selectively couples an interface node 555 to the termination voltage (Vt) according to a control line 528. The pullup 540 comprises transistors 542, 544 and 546, which are P channel transistors and selectively couple the interface node 555 to Vt according to a control bus 524 (Column 7, lines 51-60).

Thus, Ilkbahar fails to disclose, teach or suggest a first termination resistor block having a plurality of transistors with a same logic voltage being applied to gates of the transistors of said first termination resistor block, and a second termination resistor block having a plurality of transistors with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block as recited in claims 1, 10, 19 and 23.

In addition Ilkbahar fails to disclose, teach or suggest all the features recited in claims 3, 12, and 21. Each of claims 3, 12 and 21 recite a first termination resistor block having a plurality of transistors, a gate of at least one of the transistors of said first termination resistor block being applied with a supply voltage or a voltage of said transmission line.

Ilkbahar merely discloses that three pullup termination resistor blocks are selected and operated by gate signals 528, 526 and 524, where a first resistor block has an NMOS transistor 560, a second pull up resistor block 530 has PMOS transistors 532 to 536, and resistor block 540 has NMOS transistors 542 to 546 (Column 7, line 51-

Column 8, line 5).

Ilkbahar also discloses that in order to drive a low voltage, the control circuit enables the pulldown 550 and disables the pullups 530, 540 and 560. To drive the high voltage, the control circuit enables the pullup 530 and disables the pulldown 550. The control circuit 520 enables the pullup 560 and the pullup 540 to terminate the interface node 555 unless the pulldown is enabled. The control circuit 520 may be configured to disable the termination pullups 540 and 560 at other times (Column 8, lines 49-59).

In the combination of termination resistor blocks having a plurality of transistors disclosed in Ilkbahar there is no disclosure, teaching or suggestion that different logic voltages are applied to any of the termination resistor blocks as recited in amended claims 1, 10, 19 and 23 nor is there any disclosure, teaching or suggestion of a first termination resistor block having a plurality of transistors, a gate of at least one of the transistors of said first termination resistor block being applied with a supply voltage or a voltage of said transmission line as recited in amended claims 3, 12 and 21. Thus claims 1, 3,10, 12, 19, 21 and 23 are patentable over Ilkbahar.

Claims 2, 4, 6, 8, 9, 11, 13, 15, 17, 18, 20 and 22 depend from the above claims respectively therefore they are also patentable for at least the reasons recited above and for the additional features recited therein. Thus, withdrawal of the rejection of claims 1-4, 6, 8-13, 15 and 17-23 under 35 U.S.C. §102(e) is respectfully requested.

Claims 5, 7, 14 and 16 have been rejected under 35 U.S.C. §103 as being unpatentable over Ilkbahar. The rejection is respectfully traversed because Ilkbahar fails to disclose teach or suggest all the features recited in the rejected claims.

For example, Ilkbahar fails to disclose, teach or suggest all the features recited in

claims 5 and 14. Claims 5 and 14 recite a first termination resistor block having a plurality of transistors of a same conductivity type, a second termination resistor block, which differs in configuration from the first termination resistor block, wherein the first termination resistor block operates and maintains a specific resistance value when a signal of said transmission line is near a supply voltage. In addition claim 14 recites a second termination resistor block that comprises a first conductivity type transistor which does not operate near a first supply voltage, and a second conductivity type transistor which does not operate near a second supply voltage.

Ilkbahar merely discloses an embodiment wherein the pullups 530 and 540 and the pulldown 560 each comprise sixteen individual transistors which are empirically chosen but predominantly depend on the bus impedance, the desired power consumption, and the characteristics of the devices being used. In the embodiment shown in Ilkbahar the transistor 560 is not split into multiple transistors, since only a small N channel transistor is needed to provide the appropriate total termination. However, Ilkbahar discloses that the transistor 560 could be split into a plurality of transistors (Column 9, lines 1-11).

However, there is no disclosure by Ilkbahar of a first termination resistor block that operates and maintains a specific resistance value when a signal of said transmission line is near a supply voltage and a second termination resistor block comprises a first conductivity type transistor which does not operate near a first supply voltage, and a second conductivity type transistor which does not operate near a second supply voltage as recited in amended claims 5 and 14.

Thus, claims 5 and 14 are patentable over Ilkbahar. Thus withdrawal of the

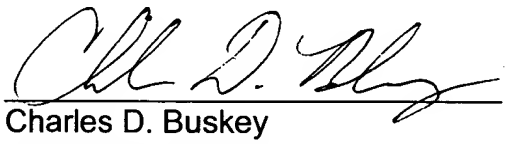
rejection claims 5 and 14 under 35 U.S.C. §103 is respectfully requested.

Claims 7 and 16 depend from claims 4 and 13 respectively. Consequently, claims 7 and 16 are patentable for at least the same reasons as claims 4 and 13 as discussed above and for the additional features recited therein. Thus, withdrawal of the rejection of claims 7 and 16 under 35 U.S.C. §103 is respectfully requested.

Should the Examiner feel that further action is required to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension time period. Any fees for such an extension of time, together with any additional fees, may be charged to counsel's Deposit Account No. 01-2300 making reference to Attorney Docket No. 100021-00062.

Respectfully submitted,



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Enclosures:
Marked-Up Version of the Claims
Abstract of the Disclosure

MARKED-UP VERSION OF THE CLAIMS

1. (Amended) A termination resistor circuit, provided in an interface circuit through which signals are transferred, comprising:

a first termination resistor block having a plurality of transistors with a same logic voltage being applied to gates of the transistors of said first termination resistor block ; and

a second termination resistor block having a plurality of transistors with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block, and wherein:

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

2. (Amended) The termination resistor circuit as claimed in claim 1, wherein:

said first termination resistor block [is of a symmetric load configuration comprising] comprises transistors of [the] a same conductivity type; and

said second termination resistor block [is of a transfer gate configuration comprising] comprises transistors of different conductivity types.

3. (Amended) [The] A termination resistor circuit [as claimed in claim 1, wherein] provided in an interface circuit through which signals are transferred via a transmission line, comprising:

[said] a first termination resistor block [comprises a first transistor and a second transistor, both being of a first conductivity type] having a plurality of transistors, a gate of at least one of the transistors of said first termination resistor block being applied with a supply voltage or a voltage of said transmission line; and

[said] a second termination resistor block [comprises a third transistor of the first conductivity type and a fourth transistor of a second conductivity type which differs from said first conductivity type] having a plurality of transistors, and which differs in configuration from said first termination resistor block, and wherein,

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

4. (Amended) The termination resistor circuit as claimed in claim 3, wherein:

[a plurality of said first termination resistor blocks and a plurality of said second termination resistor blocks are respectively arranged in parallel, and said plurality of first termination resistor blocks and said plurality of second termination resistor blocks are respectively connected for control in an arbitrary manner]

said first termination resistor block comprises transistors of a same conductivity type; and

said second termination resistor block comprises transistors of different conductivity types.

5. (Amended) [The] A termination resistor circuit [as claimed in claim 4,

wherein said first and second transistors are chosen to substantially be equal in size for each of said first termination resistor blocks so that said plurality of first termination resistor blocks have the same weight] provided in an interface circuit through which signals are transferred via a transmission line comprising:

a first termination resistor block having a plurality of transistors of a same conductivity type; and

second termination resistor block, which differs in configuration from said first termination resistor block, wherein

said first termination resistor block operates and maintains a specific resistance value when a signal of said transmission line is near a supply voltage; and

said second termination resistor block comprises a first conductivity type transistor which does not operate near a first supply voltage, and a second conductivity type transistor which does not operate near a second supply voltage, and

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

6. (Amended) The termination resistor circuit as claimed in claim 4, wherein said first and second transistors are chosen to have [an appropriate] a size for each of said first termination resistor blocks so that said plurality of first termination resistor blocks have respectively chosen [appropriate] weights.

8. The termination resistor circuit as claimed in claim 4, wherein said third and fourth transistors are chosen to have [an appropriate] a size for each of said second

termination resistor blocks so that said plurality of second termination resistor blocks have respectively chosen [appropriate] weights.

10. (Amended) A signal transmission system comprising:

a transmitting circuit for transmitting a signal;

a transmission line for transmitting the signal output from said transmitting circuit;

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor circuit comprises:

a first termination resistor block having a plurality of transistors with a same logic voltage being applied to gates of the transistors of said first termination resistor block ; and

a second termination resistor block having a plurality of transistors with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block, and wherein:

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

11. (Amended) The signal transmission system termination as claimed in claim 10, wherein:

said first termination resistor block [is of a symmetric load configuration comprising] comprises transistors of [the] a same conductivity type; and

said second termination resistor block [is of a transfer gate configuration comprising] comprises transistors of different conductivity types.

12. (Amended) [The] A signal transmission system [as claimed in claim 10, wherein] comprising:

a transmitting circuit for transmitting out a signal;

a transmission line for transmitting therethrough the signal output from said transmitting circuit;

a receiving circuit for receiving the signal transmitted from said transmitting circuit through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor comprises:

[said] a first termination resistor block [comprises a first transistor and a second transistor, both being of a first conductivity type] having a plurality of transistors, a gate of at least one of the transistors of said first termination resistor block being applied with a supply voltage or a voltage of said transmission line; and

[said] a second termination resistor block [comprises a third transistor of the first conductivity type and a fourth transistor of a second conductivity type which differs from said first conductivity type] having a plurality of transistors, which differs in configuration from said first termination resistor block, and wherein,

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

13. (Amended) The signal transmission system as claimed in claim 12, wherein,

[a plurality of said first termination resistor blocks and a plurality of said second termination resistor blocks are respectively arranged in parallel, and said plurality of first termination resistor blocks and said plurality of second termination resistor blocks are respectively connected for control in an arbitrary manner]

said first termination resistor block comprises transistors of a same conductivity type; and

said second termination resistor block comprises transistors of different conductivity types.

14. (Amended) [The] A signal transmission system [as claimed in claim 13, wherein said first and second transistors are chosen to be substantially equal in size for each of said first termination resistor blocks so that said plurality of first termination resistor blocks have the same weight.] comprising:

a transmitting circuit for transmitting out a signal;

a transmission line for transmitting therethrough the signal output from said transmitting circuit;

a receiving circuit for receiving the signal transmitted from said transmitting circuit through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination

resistor circuit comprises:

a first termination resistor block having a plurality of transistors of a same conductivity type; and

a second termination resistor block, which differs in configuration from said first termination resistor block, and wherein:

said first termination resistor block operates and maintains a specific resistance value when a signal of said transmission line is near a supply voltage; and

said second termination resistor block comprises a first conductivity type transistor which does not operate near a first supply voltage, and a second conductivity type transistor which does not operate near a second supply voltage, and wherein,

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

15. The signal transmission system as claimed in claim 13, wherein said first and second transistors are chosen to have [an appropriate] a size for each of said first termination resistor blocks so that said plurality of first termination resistor blocks have respectively chosen [appropriate] weights.

17. The signal transmission system as claimed in claim 13, wherein said third and fourth transistors are chosen to have [an appropriate] a size for each of said second termination resistor blocks so that said plurality of second termination resistor blocks have respectively chosen [appropriate] weights.

19. (Amended) A signal transmission system comprising:

a transmission line for transmitting a signal;

a receiving circuit for receiving the signal transmitted through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor circuit comprises:

a first termination resistor block having a plurality of transistors with a same logic voltage being applied to gates of the transistors of said first termination resistor block; and

a second termination resistor block having a plurality of transistors with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block, and wherein:

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

20. (Amended) The signal transmission system termination as claimed in claim 19, wherein:

said first termination resistor block [is of a symmetric load configuration comprising] comprises transistors of [the] a same conductivity type; and

said second termination resistor block [is of a transfer gate configuration comprising] comprises transistors of different conductivity types.

21. (Amended) [The] A signal transmission system [as claimed in claim 19, wherein] comprising:

a transmission line for transmitting a signal;

a receiving circuit for receiving the signal transmitted through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor circuit comprises:

[said] a first termination resistor block [comprises a first transistor and a second transistor, both being of a first conductivity type] having a plurality of transistors, a gate of at least one of the transistors of said first termination resistor block being applied with a supply voltage or a voltage of said transmission line; and

[said] a second termination resistor block [comprises a third transistor of the first conductivity type and a fourth transistor of a second conductivity type which differs from said first conductivity type] having a plurality of transistors, which differs in configuration from said first termination resistor block, and wherein,

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.

22. (Amended) The signal transmission system as claimed in claim 21, wherein,

[a plurality of said first termination resistor blocks and a plurality of said second

termination resistor blocks are respectively arranged in parallel, and said plurality of first termination resistor blocks and said plurality of second termination resistor blocks are respectively connected for control in an arbitrary manner]

said first termination resistor block comprises transistors of a same conductivity type; and

said second termination resistor block comprises transistors of different conductivity types.

23. (Amended) A signal transmission system comprising:

a transmitting circuit for transmitting out a signal;

a transmission line for transmitting therethrough the signal output from said transmitting circuit;

a receiving circuit for receiving the signal transmitted from said transmitting circuit through said transmission line; and

a termination resistor circuit connected to said transmission line and provided in an interface circuit through which signals are transferred, wherein said termination resistor circuit comprises:

a first termination resistor block having a plurality of transistors, the same logic voltage being applied to gates of the transistors of said first termination resistor block; and

a second termination resistor block having a plurality of transistors with different logic voltages being applied to gates of the transistors of said second termination resistor block, which differs in configuration from said first termination resistor block, and

wherein:

said termination resistor circuit is switched between said first termination resistor block and said second termination resistor block.